PARAMETERIZED LAYOUT SYNTHESIS OF A CMOS-COMPATIBLE SCANNING MICROMIRROR WITH ELECTROTHERMAL ACTUATION AND BIMODAL RESONANT BEHAVIOR

SÍNTESIS DE PARÁMETROS DE DISEÑO DE UN MICROESPEJO DE ESCANEADO COMPATIBLE CMOS CON ACTUACIÓN ELECTROTÉRMICA Y COMPORTAMIENTO RESONANTE BIMODAL

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ABSTRACT. This paper reports a layout synthesis methodology for design automation of a CMOS-compatible scanning micromirror with bimodal resonant behavior. The micromirror is suspended by cantilever, out-of-plane thermal bimorph actuators. Thickness optimization and scanning at second resonance is proposed to overcome the trade-off between the static and dynamic performance of the device. The objective is to automatically obtain the device layout that concurrently maximize the rotation angle, minimize the power consumption and satisfies both fabrication constraints of a standard CMOS process and high-level specifications for position of rotation axis at second resonance, scan frequency and maximum actuation voltage. The methodology uses an intermediate-level design space, defined by the thermal-to-electrical resistance ratio at room temperature of the device, to couple the constraints for maximum thermal stress and maximum current density of CMOS materials. The function evaluation procedure is developed based on a lumped element model of thermal resistance to systematically explore the design space using parametric variations of layout parameters. The methodology is applied to design a microscanner which has applications in optical coherence imaging systems. The performance of the synthesized microscanner is verified by finite element method simulations. Comparison between numerically obtained result and high-level specifications shows a good fit.

KEYWORDS: Microsystems, multiphysics modeling, CMOS-compatible micromachining, design methodology, optimal design automation, optical imaging.

RESUMEN. Este trabajo presenta una metodología de síntesis de parámetros para la automatización del diseño de un microespejo de escaneado compatible CMOS con comportamiento resonante bimodal. El microespejo está suspendido por actuadores térmicos bimorfos en voladizo con accionamiento fuera del plano. La metodología propone la optimización de espesores y el escaneo en el segundo modo de resonancia como estrategias para superar el conflicto característico entre el desempeño estático y dinámico del dispositivo. El objetivo es obtener automáticamente los parámetros de diseño del dispositivo que, de manera concurrente, maximizan el ángulo de rotación, minimizan el consumo de energía y satisfacen tanto las limitaciones de fabricación de un proceso CMOS estándar como las especificaciones de alto nivel para la posición del eje de rotación en el segundo modo de resonancia, la frecuencia de escaneado y el voltaje máximo de actuación. La metodología utiliza un espacio de diseño de nivel intermedio, definido por la razón de resistencia térmica a resistencia eléctrica del dispositivo a temperatura ambiente, para acoplar las restricciones del esfuerzo térmico máximo con la densidad de corriente eléctrica máxima de los materiales CMOS. El procedimiento de evaluación de funciones objetivos se desarrolla sobre la base de un modelo de elementos concentrados de la resistencia térmica del dispositivo para explorar sistemáticamente el espacio de diseño utilizando variaciones paramétricas. La metodología se aplica para diseñar un microescáner que tiene aplicaciones en sistemas imagenológicos de coherencia óptica. El desempeño del microescáner sintetizado es verificado por simulaciones mediante el método de elementos finitos. Los resultados obtenidos numéricamente presentan un buen ajuste con las especificaciones de alto nivel.

PALABRAS CLAVE: Microsistemas, modelado multifísico, micromaquinado compatible con CMOS, metodología de diseño, automatización de diseño óptimo, imagenología óptica.

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Introduction

The design of microelectromechanical systems (MEMS) is deeply influenced by their multiphysics nature and hybrid microfabrication processes. These heterogeneous characteristics of MEMS complicate the development of a general design methodology and introduce technological capabilities as driving factors of the design task. A MEMS design methodology that is driven by technological capabilities is very specific in applicability and usually depends on an analytic approach to determine the design parameters that fulfill the fabrications constraints and performance requirements. The analytic approach to MEMS design implies long development cycles which do not necessary lead to optimal solutions. Moreover, it lacks of systematic procedures and commonly relies on designer's experience or on trial-and-error procedures.

Several authors have proposed structured design methodologies to speed up MEMS conceptions [1-4]. In [1] the layout synthesis of electrostatic lateral resonators fabricated in surface-micromachining polyMUMPS technology is demonstrated. The designed devices using this methodology satisfy the high-level specifications for resonant frequency, quality factor and displacement amplitude at resonance. The methodology allows minimizing the device area and actuation voltage or maximizing the displacement amplitude at resonance. In [2, 3] the entire development cycle of a capacitive lateral accelerometer fabricated in CMOS technology is automated. The methodology includes tools for layout synthesis, extraction and verification. The designed device meets the sensitivity specification and has minimum thermomechanical noise. In [4] a design methodology for electrostatic torsion micromirrors fabricated in bulk-micromachining technology is presented. The performance requirements for the device include resonant frequency, pull-in angle and actuation voltage. The methodology deals with micromirrors suspended by straight-bar and serpentine-shape torsion beams and can be applied to perform design optimization and performance characterization. However, although previous papers have successfully demonstrated structured, automated and optimal methodologies to design complex MEMS, to our knowledge, serious work on layout synthesis of electrothermal actuators with out-of-plane displacement has yet to be published.

Since the fabrication feasibility of deflectable micromirrors actuated by out-of-plane thermal bimorph actuators (TBAs) was demonstrated using CMOS technology [5], similar devices have been extensively applied as resonant microscanners in optical coherence tomography (OCT) systems [6–11] and optical coherence microscopy (OCM) systems [12-15]. However, in all these designs the layout refinement phase was driven by an analytic approach based on experimentation. Therefore, the layout synthesis of these devices could help to shorten the development cycle of OCT/OCM imaging systems and increase the classes of MEMS that can be automatically designed.

This paper presents the technological implementation and analytical modeling of a CMOS-compatible resonant microscanner with dual scanning mode in order to develop a layout synthesis methodology that automates its design. The device consists of a movable micromirror suspended by cantilever TBAs. Scanning at second resonance is investigated as a strategy to increase the scan frequency of the device and to keep stationary the reflection point. The design objective of the synthesis methodology is to automatically obtain a layout configuration that satisfies the high-level specifications for position of rotation axis at second resonance, scan frequency and maximum actuation voltage of the device. In addition, a high rotation angle and low power consumption are required during static operation. Furthermore, design parameters must meet the fabrication constraints of CMOS technology. Our approach to solve the layout synthesis problem is to use an intermediate-level design space defined by the ratio of thermal to electrical resistance at room temperature of the device. As we shall describe, this design space has physical meaning and can be

easily related to the geometry and materials properties of the device. Parametric exploration of the design space is performed using a monotonic objective function based on a lumped element model (LEM) of thermal resistances.

Description of the scanning micromirror

The microscanner designed in this paper allows modifying the angular position of an incident laser beam over a one-dimensional direction. The operation principle of the device is based on the out-of-plane deflection of a movable micromirror suspended by cantilever TBAs. This class of scanners is characterized by their high deflection angles, high scan rates, very high optical efficiencies, good long-term stabilities, two-dimensional scanning capabilities and wavelength independence [16].

Device structural components: The device topology includes a square mirror plate suspended by an array of parallel cantilever beams with rectangular geometry as illustrated in figure 1(a). Previous experimental work reported in [10, 11] has demonstrated that this beams arrangement eliminates the adverse hysteresis effect caused by thermal relaxation and wobbling occurred in earlier designs [6-9]. In this topology, the minimum resistors width W_r as well as the minimum beams width W_b are set by the design rules of the fabrication technology and the number of supporting beams n_b depends on the length of the mirror plate L_m, such that $n_b = L_m / W_m$.

Figure 1(b) exposes the composite structure of the device which contains a high reflective metal layer stacked over a bottom material layer. In addition, a set of U-shaped heating resistors are embedded within the bottom layer of each beam to form the electrothermal actuation system. This way, an out-of-plane deflection is achieved as a result of the dissimilar thermoelastic response of composing layers to Joule heating phenomenon.

The positions of rotation axes at resonance, denoted as r_1 and r_2 in figure 1(b), are determined by the nodes of the first two transversal vibration modes and thus the axes are accessible when the device is excited at its first and second resonant frequency, respectively.

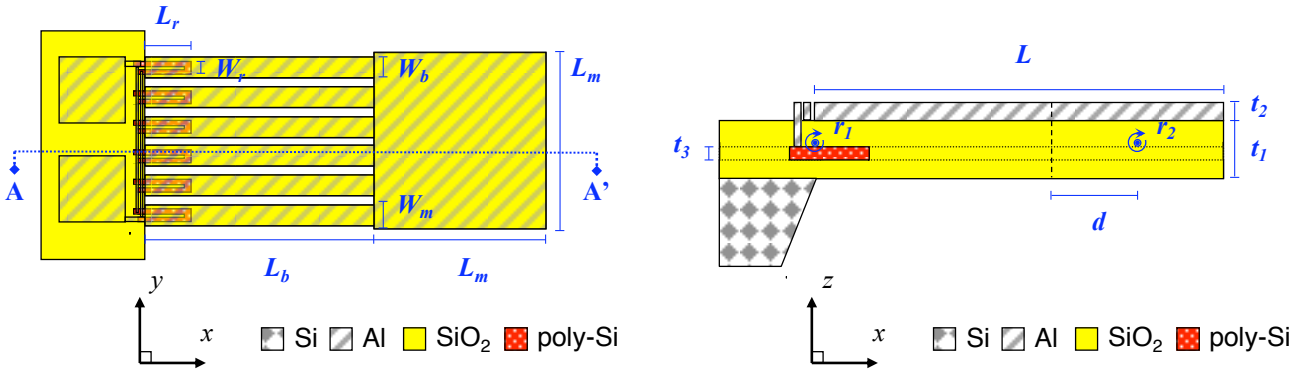

Figure 1. Schematic representations of the scanning micromirror: (a) top view with translucent layers and (b) cross-sectional view along the plane A-A'.

Device implementation in CMOS technology: In this particular design, the selected materials for the microscanner are taken from a 0.6 μm CMOS process, due to its Metal/Oxide stacking sequence and physical properties of the involved materials, and the design parameters are subjected to the process and

design rules constraints of this technology. The 0.6 μm CMOS process involves six structural layers plus a passivation layer used for electrical isolation of electronic components. The name, material and thickness of each structural layer are shown in table 1. From table 1 it is possible to extract three different stacking sequences to implement the device concept in CMOS technology. The three sequences share a basic configuration comprising the POLY1 layer embedded within the first two layers of SiO2, namely FOX and ILD. Stacked to this basic configuration can be the MET1 layer, the MET1 and MET2 layers or the IMD1 and MET2 layers. Each combination represents a different stacking sequence to form the reflective surface of the microscanner. Depending on the numbers of employed layers, the thickness of the bottom and top layers of the composite structure, denoted as t_1 and t_2 in figure 1(b), can only take the discrete values summarized in table 2.

Table 1. Structural layers available in the 0.6 μm CMOS process.

Name	Material	Index	Thickness, t_i (nm)		
			Minimum	Typical	Maximum
MET2	Al	2,2	800	940	1080
IMD1	SiO_2	1,3	570	650	750
MET1	Al	2,1	600	720	840
ILD	SiO_2	1,2	500	650	750
POLY1	poly-Si	3	230	250	270
FOX	SiO_2	1,1	350	400	450

The layers are listed from last to first as deposited during the process.

Table 2. Feasible typical thicknesses for different CMOS stacking sequences.

Layer	Material	Index	First stacking sequence		
			Composing layers	Typical thickness, t_i (nm)	Typical thickness ratio, t_2 / t_1
Top	Al	2	MET1	$t_2 = t_{2,1} = 720$	$t_2 / t_1 = 0.69$
Bottom	SiO_2	1	FOX and ILD	$t_1 = t_{1,1} + t_{1,2} = 1050$	
Layer	Material	Index	Second stacking sequence		
			Composing layers	Typical thickness, t_i (nm)	Typical thickness ratio, t_2/t_1
Top	Al	2	MET1 and MET2	$t_2 = t_{2,1} + t_{2,2} = 1660$	$t_2 / t_1 = 1.58$
Bottom	SiO_2	1	FOX and ILD	$t_1 = t_{1,1} + t_{1,2} = 1050$	
Layer	Material	Index	Third stacking sequence		
			Composing layers	Typical thickness, t_i (nm)	Typical thickness ratio, t_2/t_1
Top	Al	2	MET2	$t_2 = t_{2,2} = 940$	$t_2 / t_1 = 0.55$
Bottom	SiO_2	1	FOX, ILD and IMD1	$t_1 = t_{1,1} + t_{1,2} + t_{1,3} = 1700$	

Analytical model

The symmetry of the beams arrangement allows to discretize the whole device structure into a finite number of TBAs in order to simplify its analysis. Moreover, when the spatial period of the beams in the array is restricted to be approximately equal to the beams width, i.e. $W_m \approx W_b$, the overall structure of the microscanner can be modeled without loss of generally as a single TBA [17]. The modeled TBA is composed of a prismatic cantilever beam of length $L = L_b + L_m$, width W_b and thickness $t = t_1 + t_2$.

Relevant physical properties of CMOS materials are summarized in table 3. The data of table 3 is used throughout the subsequent modeling process to qualitatively and quantitatively describe the static and dynamic behavior of the CMOS-compatible TBA in response to constant and periodic electrical excitation.

Table 3. Physical data of CMOS materials [18–20].

Quantity	Symbol	Units	Material		
			SiO_2 (i=1)	Al (i=2)	poly-Si (i=3)
Young's modulus	E_i	GPa	7.00×10^{1}	7.20×10^{1}	1.60×10^{2}
Poisson's ratio	ν_i		1.70×10^{-1}	3.00×10^{-1}	2.20×10^{-1}
Yield strength	Y_{oi}	MPa	8.40×10^{3}	1.70×10^{2}	2.00×10^{3}
Specific mass density	ρ_i	kg·m^{-3}	2.20×10^{3}	2.70×10^{3}	2.33×10^{3}
Coefficient of thermal expansion	α_i	K^{-1}	5.30×10^{-7}	2.36×10^{-5}	2.33×10^{-6}
Thermal resistivity	ϱ_{Ti}	m·K·W^{-1}	7.69×10^{-1}	5.56×10^{-3}	6.76×10^{-3}
Electrical resistivity	ϱ_{Ei}	Ω·m	1.00×10^{10}	2.65×10^{-8}	1.43×10^{-5}
Coefficient of thermal resistivity	β_{Ti}	K^{-1}	1.00×10^{-3}	6.35×10^{-5}	2.00×10^{-2}
Coefficient of electrical resistivity	β_{Ei}	K^{-1}	--	--	9.10×10^{-4}

The analytical model is based on the same assumptions as those in previous work [21-23] and these are summarized below:

1) The composite structure is assumed to be symmetric about the *xz* plane.
2) The temperature distribution within the composite structure is assumed to be uniform.
3) The length and width of the two layers joined in the composite structure are assumed to be equal and the layer thicknesses are assumed to be homogenous.
4) The mechanical properties of the CMOS materials are supposed to be linearly elastic, isotropic, homogenous and temperature independent.
5) The heat loss by convention and radiation is neglected.
6) The air-damping effect is neglected.
7) The initial curvature due to residual stress is neglected.

Static behavior: The static electrothermomechanical behavior of TBA is analyzed using two theoretical models. As the thermomechanical domain involves less design variables than the electrothermal domain, we begin our analysis by modeling the mechanical response of the TBA to temperature variations and then we model its thermal response to constant electrical excitations.

1) Thermomechanical model: For small deflections of the TBA, the rotation angle at any point on its deflection curve is given by [24]

$$\theta = \kappa \cdot x, \tag{1}$$

where κ is the curvature induced by a constant bending moment and x is the longitudinal coordinate.

Given that the bending moment is caused by thermal stresses resulting from temperature variations within the composite structure, by ignoring the contribution of the thin poly-Si (i=3) layer, the thermally induced curvature in the TBA is expressed by [22]

$$\kappa = \frac{6(t_1 + t_2)(\alpha_1 - \alpha_2)\Delta\bar{T}}{\frac{E_1 t_1^3}{E_2 t_2} + \frac{E_2 t_2^3}{E_1 t_1} + 4t_1^2 + 6t_1 t_2 + 4t_2^2}, \tag{2}$$

where E_i, α_i and t_i are the Young's modulus, thermal expansion coefficient and thickness of the SiO_2 (i=1) and Al (i=2) layers, respectively; and $\Delta\bar{T}$ is the average temperature variation from room temperature (assumed T_0 = 296 K) within the composite structure. The average temperature concept is introduced to approximate the ideal situation of a uniform temperature distribution. The thermal stress in the ith layer is determined by $\sigma_i = E_i \cdot \alpha_i \cdot \Delta\bar{T}$.

Now, defining the thermal sensitivity as the curvature that the TBA is able to achieve per degree kelvin, (2) shows that this performance parameter is strongly dependent on the thickness ratio of the composite structure. Numerical evaluations of (2) for different values of t_2 / t_1 are plotted in figure 2. Figure 2 shows that the TBA reaches its maximum curvature when t_2 / t_1 = 0.49. However, the feasible thicknesses with the assumed 0.6 μm CMOS process impose a new discrete design space from which the exact optimal solution cannot be obtained. Therefore, since the closer feasible solution to the optimal thickness ratio that maximizes the thermal sensitivity is achieved when the microscanner is designed according to the third staking sequence presented in table 2, a thickness ratio of t_2 / t_1 = 0.55 is assumed for the rest the analysis.

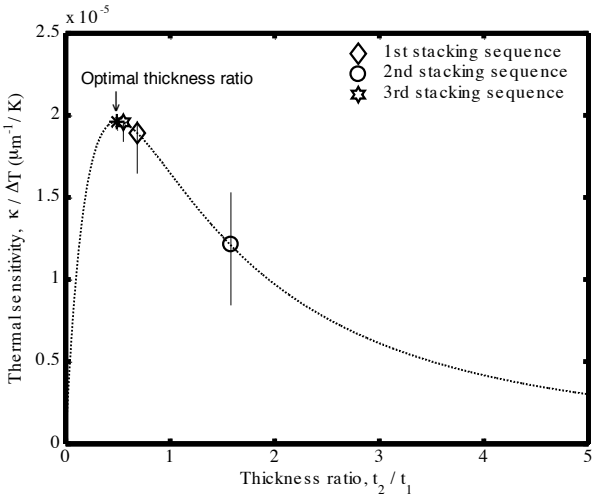

Figure 2. Thermal sensitivity of the CMOS-compatible thermal bimorph actuator. Typical values and error bars are shown for each stacking sequence.

2) Electrothermal model: The average temperature increment above room temperature within the poly-Si resistor is described by its thermal resistance to ambient R_T and the dissipated power P_D as [25]

$$\Delta\bar{T}_3 = R_T \cdot P_D = R_T \cdot V_a^2 / R_3, \tag{3}$$

where V_a is the actuation voltage and R_3 is the electrical resistance in the poly-Si layer whose value is determined by $R_3 = \varrho_{E3} \cdot L_{eff} / (t_3 \cdot W_{eff})$, where ϱ_{E3} is the electrical resistivity of the poly-Si layer, L_{eff} is the effective length over which the resistance is measured, t_3 is the thickness of the poly-Si layer and W_{eff} is the effective width of the resistor path.

Now, we introduce a design parameter defined by the ratio of thermal to electrical resistance R_{TE} in order to model the dependence of resistances to temperature. R_{TE} has the units of $\mathrm{K}\cdot\mathrm{W}^{-1}\cdot\Omega^{-1}$ and it is defined as

$$R_{TE} \equiv \frac{R_T}{R_3} = R_{TE0}\left(\frac{1+\beta_T\cdot\Delta\overline{T}}{1+\beta_{E3}\cdot\Delta\overline{T}_3}\right), \tag{4}$$

where R_{TE0} is the ratio of R_T to R_3 at room temperature, β_{E3} is the linear coefficient of electrical resistivity of the poly-Si layer and β_T is the linear coefficient of thermal resistivity of the composite structure whose value is determined by $\beta_T = (\varrho_{T1}\cdot t_2\cdot\beta_{T2} + \varrho_{T2}\cdot t_1\cdot\beta_{T1}) / (\varrho_{T1}\cdot t_2 + \varrho_{T2}\cdot t_1)$, where ϱ_{Ti} and β_{Ti} are the thermal resistivity and coefficient of thermal resistivity of the *i*th layer, respectively. Note from table 3 that typical values for β_{E3} and β_T are 9.10×10^{-4} K^{-1} and 7.56×10^{-5} K^{-1}, respectively.

The temperature distributions in (4) were calculated in [17] as

$$\Delta\overline{T}_3 \approx \frac{1}{L_r}\int_0^{L_r}\Delta T_3(x)dx = \varrho_T\cdot\varrho_{E3}\cdot J^2\cdot L_r\left(\frac{3L-2L_r}{3}\right) \tag{5}$$

and

$$\Delta\overline{T} \approx \frac{1}{L-L_r}\int_{L_r}^{L}\Delta T(x)dx = \varrho_T\cdot\varrho_{E3}\cdot J^2\cdot L_r\left(\frac{L-L_r}{2}\right), \tag{6}$$

where J is the linear current density in the poly-Si layer whose value is determined by $J = V_a / (R_3\cdot L_{eff})$.

In (5) and (6), $\Delta T_3(x)$ and $\Delta T(x)$ are the steady-state, one-dimensional solutions to the heat conduction equation for both, non-homogeneous and homogeneous cases. This is

$$\frac{d^2\Delta T}{dx^2} = \begin{cases} -\ \varrho_T\cdot\varrho_{E3}\cdot J^2 & 0 < x \le L_r \\ 0 & L_r < x \le L \end{cases} \tag{7}$$

subjected to the boundary conditions: $\mathrm{d}\Delta T_3(0)/\mathrm{d}x = 0$ and $\Delta\mathrm{T(L)} = 0$; and having the continuity conditions: $\Delta T_3(L_r) = \Delta T(L_r)$ and $\mathrm{d}\Delta T_3(L_r)/\mathrm{d}x = \mathrm{d}\Delta T(L_r)/\mathrm{d}x$.

Although long heating resistors are needed for decreasing the power consumption, we assume a short poly-Si resistor, i.e. $L_r << 0.13L$, in order to concentrate the maximum temperature distribution near the bending axis of the TBA and thus preserving the mirror flatness. Then, from (5) and (6), we obtain

$$\Delta\overline{T} \approx \frac{1}{2}\Delta\overline{T}_3. \tag{8}$$

Finally, by substituting (3) and (8) into (4), $\Delta\overline{T}$ can be rewritten in polynomial form as

$$4\cdot\beta_{E3}\cdot\Delta\overline{T}^2 + (2-\beta_T\cdot R_{TE0}\cdot V_a^2)\Delta\overline{T} = R_{TE0}\cdot V_a^2. \tag{9}$$

The variation of $\Delta\overline{T}$ as a function of V_a is plotted in figure 3 for different values of R_{TE0}. We can see in figure 3 that, for a fixed value of V_a, the poly-Si resistor generates more heat when the value of R_{TE0} increases. Therefore, R_{TE0} can be used as an indicator of the device efficiency to transform electrical into thermal energy. However, high values of $\Delta\overline{T}$ will result in thermal stresses beyond the elastic limit of materials, i.e. $\sigma > Y_\sigma$, where Y_σ is the yield strength. Consequently, an adequate value of R_{TE0} is required in order to generate a tolerable heating in the structure.

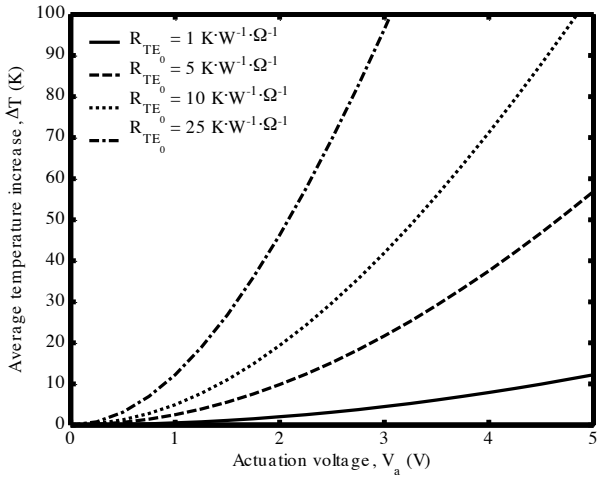

Figure 3. Average temperature increase within a CMOS-compatible thermal bimorph actuator designed according to the 3rd stacking sequence.

Dynamic behavior: The dynamic mechanical behavior of the TBA is analyzed using the Euler-Bernoulli beam theory. First, we perform a modal analysis of the TBA, and then, we find geometric relations that allow us to position the second node of the second transversal vibration mode at a fixed coordinate along the mirror length.

1) Modal analysis: Transversal mode shapes are obtained by solving the one-dimensional Euler-Bernoulli equation [26]

$$\hat{E}\cdot I\frac{\partial^4 w}{\partial x^4}+\overline{\rho}\cdot A\frac{\partial^2 w}{\partial t^2}+\gamma\frac{\partial w}{\partial t}=F(t), \tag{10}$$

where $\overline{\rho}$ and A are the average specific mass density and cross sectional area of the TBA, respectively; γ is the damping coefficient of the medium and $F(t)$ is the driving load due to a periodic excitation. The value of $\overline{\rho}$ is determined by $\overline{\rho} = (\rho_1 \cdot t_1 + \rho_2 \cdot t_2) / (t_1 + t_2)$, where ρ_i is the specific mass density of the ith layer. For this TBA, $\hat{E}\cdot I = \hat{E}_1\cdot I_1 + \hat{E}_2\cdot I_2$ and $\hat{E}_i = E_i/\left(1-\nu_i^2\right)$, where ν_i is the Poisson's ratio of the ith layer and I_i is the moment of inertia of the ith layer with respect to the neutral axis. I_1 and I_2 are given by

$$I_1=\frac{W_b\cdot t_1}{12}\left(E_1^2\cdot t_1^4+2E_1\cdot t_1^3\cdot E_2\cdot t_2+4t_1^2\cdot E_2^2\cdot t_2^2+6t_1E_2^2t_2^3+3E_2^2\cdot t_2^4\right), \tag{11}$$

$$I_2 = \frac{W_b \cdot t_2}{12}\left(E_2^2 \cdot t_2^4 + 2E_2 \cdot t_2^3 \cdot E_1 \cdot t_1 + 4t_2^2 \cdot E_1^2 \cdot t_1^2 + 6t_2 E_1^2 t_1^3 + 3E_1^2 \cdot t_1^4\right), \tag{12}$$

Equation 10 is subjected to the following boundary conditions that are satisfied at all time t: $w(0,t) = 0$, $\partial w(0,t)/\partial x = 0$, $\partial^2 w(L,t)/\partial x^2 = 0$ and $\partial^3 w(L,t)/\partial x^3 = 0$. Then, for the case of an undamped system with free oscillations, the nth transversal mode shape normalized to the maximum amplitude of vibration is given by [26]

$$\overline{w}_n(\bar{x}) = \frac{1}{2}\left\{\cosh(\xi_n \bar{x}) - \cos(\xi_n \bar{x}) + \psi_n\left[\sin(\xi_n \bar{x}) - \sinh(\xi_n \bar{x})\right]\right\}, \tag{13}$$

where $\bar{x}$ is the longitudinal coordinate x normalized to L, $\psi_n = \left[\cosh(\xi_n) + \cos(\xi_n)\right]/\left[\sinh(\xi_n) + \sin(\xi_n)\right]$ and ξ_n is a dimensionless constant determined by the following eigenvalue equation

$$1 + \cos(\xi_n) \cdot \cosh(\xi_n) = 0. \tag{14}$$

Numerical solution to (14) and to (13) were obtained in [27] for $n = 2$ as $\xi_2 = 4.6941$ and $\bar{r}_2 = 0.7834$, where $\bar{r}_2$ is the normalized position of the second node of the second transversal vibration mode.

The nth natural frequency of the TBA is approximately given by [28]

$$f_n \approx \frac{1}{2\pi}\left(\frac{\xi_n}{L}\right)^2 \sqrt{\frac{\hat{E}_1 \cdot I_1 + \hat{E}_2 \cdot I_2}{\overline{\rho} \cdot A}}. \tag{15}$$

2) Position of rotation axes at resonance: From geometrical relations shown in figure 1(b), the position of the rotation axis at second resonance r_2 can be expressed in terms of the beam length L_b and the scale factor d as

$$r_2 = L_b + d. \tag{16}$$

By definition, r_2 normalized to L is $\bar{r}_2 \equiv r_2/L$. Then from (16) and $\bar{r}_2$ we obtain a geometric constraint for the lengths of each section of the TBA as

$$L_b = \frac{d - \bar{r}_2 L_m}{\bar{r}_2 - 1}. \tag{17}$$

Layout synthesis

Two steps are required to automatically generate a feasible layout configuration for the microscanner from its high-level specifications. First we parameterize the layout problem in terms of objectives, variables and constraints for the design as suggested in [1] and second, we develop a function evaluation procedure to systematically explore the design space.

Throughout the analytical model section, four objective functions, four design variables and ten constraints are identified. Objective functions include the resonant frequency, rotation angle, dissipated power and ratio

of thermal to electrical resistance at room temperature of the device. Design variables and constraints are summarized in table 4 and table 5, respectively. High-level specifications include the position of rotation axis at second resonance, scan frequency and maximum actuation voltage.

Table 4. Design variables.

Discrete design variable	Expression	Value		
		1st stacking sequence	2nd stacking sequence	3rd stacking sequence
Thickness ratio	t_2 / t_1	0.69	1.58	0.55
Continuous design variables	**Symbol**	**Value**		
		Units	Minimum	Maximum
Mirror length	L_m	μm	$1.5D_{1/e}$	$10D_{1/e}$
Resistor length	L_r	μm	W_{eff}	$0.13L$
Beam width	W_b	μm	$W_r + 2\,DR_2$	L_m

Table 5. Design constraints.

Functional constraints	Symbol	Units	Typical value
Gaussian laser beam diameter	$D_{1/e}$	μm	40
Maximum thermal stress in the layer with lower yield point (Al layer)	$Y_{\sigma 2}$	MPa	170
Maximum linear current density in the poly-Si layer	J_{max}	mA/μm	0.18
Geometric constraints	**Symbol**	**Units**	**Expression**
Beam length	L_b	μm	$(d - \bar{r}_2 \cdot L_m) / (\bar{r}_2 - 1)$
Scanner length	L	μm	$L_b + L_m$
Resistor width	W_r	μm	$2W_{eff} + DR_1$
Resistor effective length	L_{eff}	μm	$2L_r + DR_1$
Design rules	**Symbol**	**Units**	**Value**
Resistor effective width	W_{eff}	μm	5.5
Resistor notch	DR_1	μm	1.32
Beam width enclosure of resistor width	DR_2	μm	3.3

We solved the layout design problem by using a two-phase synthesis approach. The first phase permits to map the high-level specifications into a less-abstract, intermediate level design space defined by the ratio of thermal to electrical resistance at room temperature of the device R_{TE0}. The synthesized value of R_{TE0} is then used as a functional constraint during the second phase which allows to completely define the low-level layout configuration that fulfills the fabrication constraints of CMOS technology and the functional constraints of CMOS materials. The second phase uses a LEM to evaluate the thermal resistance at room temperature of the device R_{T0} and thus R_{TE0}. The thermal network of the device is shown in figure 4 and its lumped elements are defined in table 6.

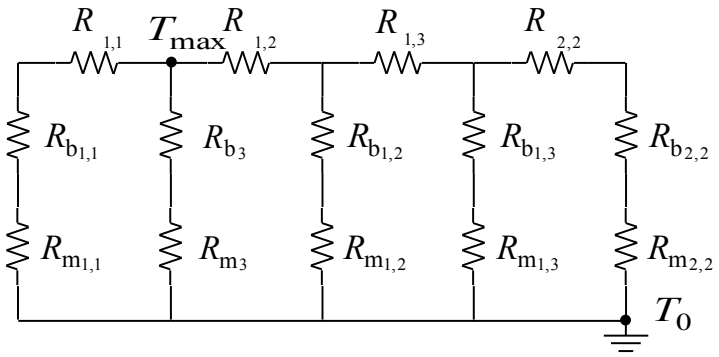

Figure 4. Lumped elements model of the thermal network of the microscanner. The model considers heat dissipation by conduction through the length and thickness of the composite structure.

Table 6. Thermal resistances of the network elements.

Layer	Index	R_i	R_{bi}	R_{mi}
MET2	2,2	$\varrho_{T2}\cdot t_{2,2} / (W_b\cdot L_r)$	$\varrho_{T2}(L_b-L_r) / (W_b\cdot t_{2,2})$	$\varrho_{T2}\cdot L_m / (W_b\cdot t_{2,2})$
IMD1	1,3	$\varrho_{T1}\cdot t_{1,3} / (W_b\cdot L_r)$	$\varrho_{T1}(L_b-L_r) / (W_b\cdot t_{1,3})$	$\varrho_{T1}\cdot L_m / (W_b\cdot t_{1,3})$
ILD	1,2	$\varrho_{T1}\cdot t_{1,2} / (W_b\cdot L_r)$	$\varrho_{T1}(L_b-L_r) / (W_b\cdot t_{1,2})$	$\varrho_{T1}\cdot L_m / (W_b\cdot t_{1,2})$
POLY1	3	$\varrho_{E3}\cdot L_{eff} / (W_{eff}\cdot t_3)$	$\varrho_{T1}(L_b-L_r) / (W_b\cdot t_3)$	$\varrho_{T1}\cdot L_m / (W_b\cdot t_3)$
FOX	1,1	$\varrho_{T1}\cdot t_{1,1} / (W_b\cdot L_r)$	$\varrho_{T1}(L_b-L_r) / (W_b\cdot t_{1,1})$	$\varrho_{T1}\cdot L_m / (W_b\cdot t_{1,1})$

All resistances have the units of $K\cdot W^{-1}$ except R_3.
R_3 has the units of Ω.

The design space is explored with parametric variations of the design variables due to the monotonicity of objective functions. The overall layout synthesis methodology is described step-by-step as follows:

First phase of layout synthesis

1) Initialize the design variable L_m to the upper limit of its design space.
2) Calculate L_b using (17) constrained with the high-level specification for the position of rotation axis at second resonance.
3) Calculate L using the geometric constraint expressed by $L = L_b + L_m$.
4) Evaluate the objective function for the resonant frequency using (15) constrained with $t_2 / t_1 = 0.55$.
5) If the error between the obtained resonant frequency and its high-level specification is less or equal than the desired tolerance, store the values of the layout parameters L_m, L_b and L. Otherwise decrease the initial value of L_m until the high-level specification for the resonant frequency is satisfied or the lower limit of its design space is reached.
6) Initialize the value of the rotation angle to a minimum value, e.g. $\theta = 0.01^o$.
7) Calculate κ using (1) constrained with $x = L_b + d$.
8) Calculate $\Delta\overline{T}$ using (2) constrained with $t_2 / t_1 = 0.55$.
9) Calculate the thermal stress in the layer with lower yield point using $\sigma_i = E_i\cdot\alpha_i\cdot\Delta\overline{T}$.
10) If $\sigma_i < Y_{\sigma i}$, increase the initial value of θ until $\sigma_i \geq Y_{\sigma i}$ is satisfied. Otherwise calculate and store R_{TE0} using (9) constrained with the high-level specification for the actuation voltage.

Second phase of layout synthesis

1) Initialize the design variable L_r to the lower limit of its design space.
2) Calculate L_{eff} using the geometric constraints expressed by $L_{eff} = 2L_r + DR_1$.
3) Calculate $R_3 = \varrho_{E3} \cdot L_{eff} / (t_3 \cdot W_{eff})$.
4) Calculate $J = V_a / (R_3 \cdot L_{eff})$.
5) If $J < J_{max}$, increase the initial value of L_r until $J \geq J_{max}$ is satisfied. Otherwise store the value of the layout parameter L_r and the value of R_3.
6) If $L_r < 0.13L$, take $L_r = 0.13L$, recalculate both L_{eff} and R_3, and store the new values of L_r and R_3.
7) Initialize the design variable W_b to the lower limit of its design space.
8) Evaluate R_{T0} using the LEM of figure 6. R_{T0} is determined by calculating the equivalent resistance of the thermal network between the nodes T_{max} and T_0.
9) Calculate $R_{TE0} = R_{T0} / R_3$.
10) If the error between the obtained R_{TE0} and its synthesized value during the first phase is less or equal than the desired tolerance, store the value of the layout parameter W_b. Otherwise increase the initial value of W_b until the tolerance criteria is satisfied or the upper limit of its design space is reached.

Case study: microscanner for OCT/OCM systems

In order to validate the layout synthesis methodology, we implemented it in an algorithm using Matlab [29]. The algorithm was used to design a microscanner for typical OCT/OCM imaging systems. Scanning at second resonance is proposed to overcome the trade-off between resonant frequency and rotation angle of the device. The rotation axis at second resonance was specified to be positioned at the center of the mirror plate, i.e. $d = 0.5L_m$, for maintaining the reflection point stationary as occurs in torsion mirrors. A resonant frequency of 50 ± 0.5 kHz was specified to exceed the performance requirements for scanning speed of most OCT/OCM systems [6–15]. The actuation voltage was specified to a typical value in CMOS electronics of 2 V to facilitate the integration of the scanner with CMOS technology. The diameter of the collimated Gaussian laser beam $D_{1/e}$ was set to 40 μm [30].

In brief, a microscanner operating at second resonance with a scan frequency of 50 ± 0.5 kHz and a rotation axis located at the center of the mirror plate is required. Additionally, the microscanner must have its maximum rotation angle and its minimum power consumption at 2 V. Moreover, its materials must behave elastically and tolerate the generated current density.

The design variables L_m, L_r and W_b were initialized to 400 μm, 5.5 μm and 18.92 μm, respectively. The step size decrement and increment were taken as 1 μm, 0.1 μm and 0.1 μm, respectively. The value of θ was initialized to 0.01° with a step size increment of 0.25°. The tolerance for both the scan frequency f_2 and the intermediate-level design parameter R_{TE0} was 1%. The evolution of the design variables, objective functions and functional constraints are shown in figure 5, figure 6 and figure 7, respectively.

In the high to intermediate-level synthesis, we monitored, for the dynamic behavior synthesis, the evolution of the length of each section of the scanner until the objective function for the second natural frequency reached its design goal, i.e. f_2, = 50 ± 0.5 kHz, as shown in figure 5 and figure 6(a); likewise, we monitored, for the static behavior synthesis, the evolution of the angle of rotation until the functional constraint for the thermal stress in the Al layer reached the plastic deformation regime, i.e. $\sigma_2 \geq Y_{\sigma 2} = 170$ MPa, as shown in figure 6(a) and figure 7.

In the intermediate to low-level synthesis, we monitored, for the electrical domain synthesis, the evolution of the resistor length until the functional constraint for the current density in the poly-Si was less than the

maximum admissible value imposed by the design rules of the CMOS process, i.e. $J \leq J_{max} = 0.18$ mA/μm, as shown in figure 5 and figure 7; the dissipated power P_D is also shown for reference in figure 6(b). Similarly, we monitored, for the thermoelectrical domain synthesis, the evolution of the beam width until the objective function for the thermal-to-electrical resistance ratio at room temperature of the device was less than the synthesized value during the first phase of layout synthesis, as shown in figure 5 and figure 6(b).

The synthesized and constrained layout parameters of the microscanner are summarized in table 7. In this table 7, the spatial period of the beams was constrained to $W_m = 39.67$ μm to allocate six TBAs in the array. Moreover, according to the analytically derived models, a scanner designed with this layout configuration has a $R_{TE0} = 55.87$ K·W^{-1}·Ω^{-1} and achieves a scanning frequency of 49.88 kHz at second resonance. Its maximum admissible average temperature increase before plastic deformation is 99.4 K ($\sigma_2 = 168.96$ MPa) and its maximum angle of rotation is 29.5° for $V_a = 2$ V considering a maximum temperature increase. The electrical resistance of such scanner is 1.5 kΩ, its thermal resistance at ambient temperature is 83.5 kK·W^{-1}, the linear current density in its poly-Si layer is 0.009 mA/μm and it dissipates 2.7 mW.

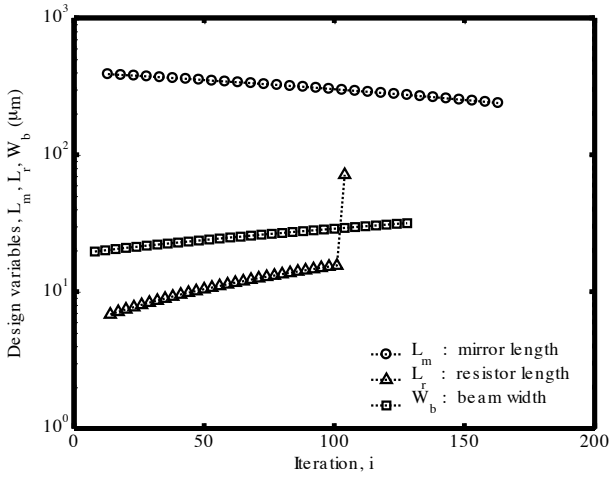

Figure 5. Evolution of design variables during the layout synthesis.

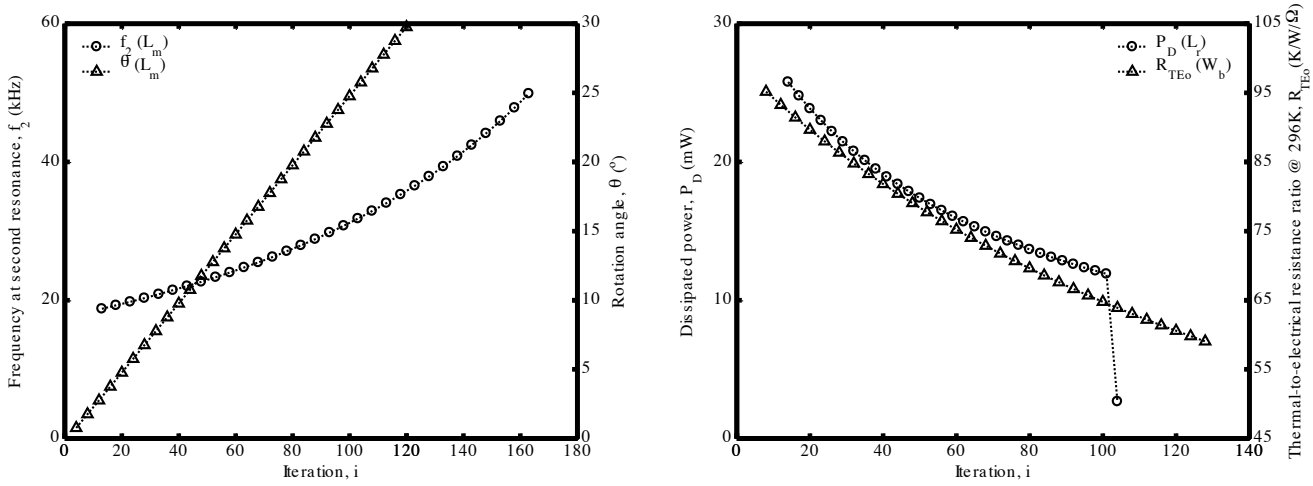

Figure 6. Evolution of objective functions during the: (a) first and (b) second phase of the layout synthesis.

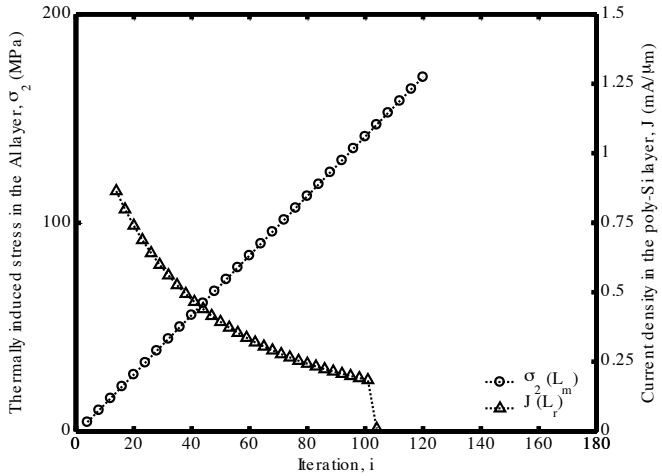

Figure 7. Evolution of functional constraints during the layout synthesis.

Table 7. Layout configuration of the microscanner.

Parameter	Synthesized value	Parameter	Constrained value
L_m	238.00 μm	L_b	311.40 μm
L_r	71.42 μm	W_r	12.32 μm
W_b	31.62 μm	W_m	39.67 μm

Design verification

The static and dynamic performance of the synthesized microscanner was verified by conducting FEM simulations in CoventorWare [31]. The numerically obtained results were compared to functional constraints and high-level specifications as well as to theoretically obtained results for validating both, the design concept, and the analytical equations.

Static performance: The static performance of the microscanner was numerically obtained by performing a parametric FEM simulation using the CoventorWare's coupled solver MemETherm. In this FEM simulation, the actuation voltage was varied from 0 to 2 V with linear increments of 0.25 V. The rotation angle at the center of the mirror plate, the linear current density in the poly-Si layer and the principal stresses in the composite structure were evaluated at each step. The analytical solution for the rotation angle was obtained using (9), (2) and (1).

The results obtained by FEM simulation and by analytical modeling are illustrated in figure 8. Figure 9 illustrates that the maximum error of 1.88° (12.82%) occurs for an actuation voltage of 1.25V. However, for the high-level specification of 2 V, both solutions have a good agreement with an error of 1.22° (4.25%). Moreover, FEM simulation shows that J = 35.1 μA/μm at 2 V and, although the error between FEM simulation and analytical solution is 26.1 μA/μm (74.35%), this value is still below J_{max}. Principal stresses obtained by FEM simulation at 2 V are 0.00 MPa, -9.28 MPa and -32.98 MPa, respectively. Thus, by considering a Von Mises Yield criterion, these values confirm that materials remain in the elastic regime. The static shape deformation of the device at 2 V is shown for reference in figure 9. These results confirm the competence of the proposed methodology to automatically design microscanners with high rotation angles and low actuation voltages that fulfills the function constraints for maximum thermal stress and

maximum linear current of CMOS materials. The results also verify the precision of the analytical equations to describe the thermomechanical response of the microscanner during static operation.

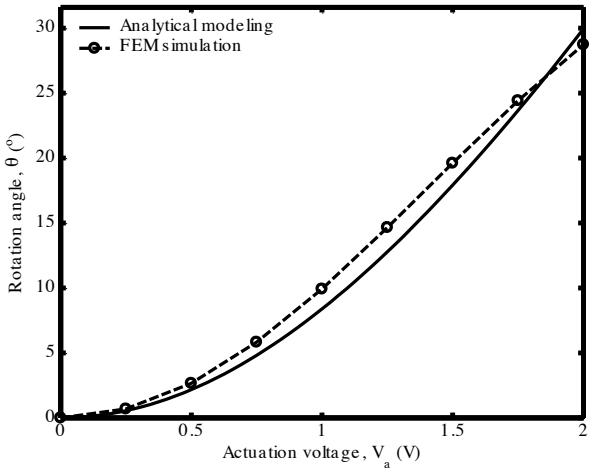

Figure 8. Deflection curve. Rotation angle obtained by analytical modeling and by FEM simulation.

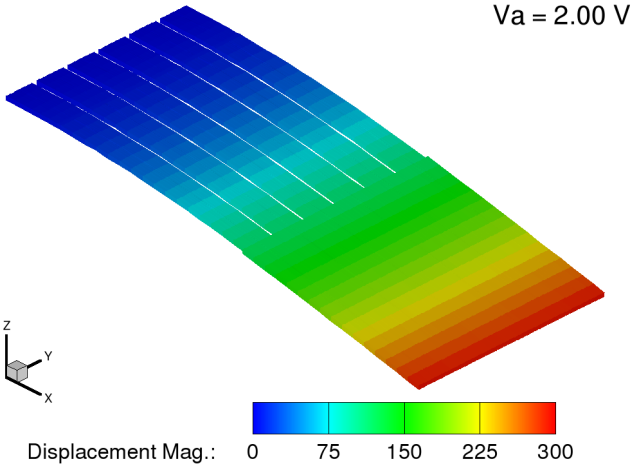

Figure 9. Static shape deformation normalized to 1 μm for an actuation voltage of 2 V.

Dynamic performance: The modal behavior of the first two vibration modes of the microscanner was numerically obtained by performing a FEM simulation using the CoventorWare's mechanical solver Mem-Mech. The analytical solution for the position of rotation axis at second resonance and resonant frequencies were obtained using (16) and (15), respectively.

The results obtained by FEM simulation and by analytical modeling are summarized in table 8. The results from table 8 show an excellent fit between the FEM simulation, high-level specification and analytical solution for the position of rotation axis at second resonance with a maximum error of 0.01 μm (0.002%). For the first resonant frequency, the error between the FEM simulation and the analytical solution is 180 Hz (2.21%). The FEM simulation, high-level specification and analytical solution are in good agreement for the second resonant frequency with a maximum error of 190 Hz which is about 0.38% of the high-level specification. The dynamic shape deformation of the device for the first two transversal modes of vibration is shown for reference in figure 10. Results from table 8 confirm the expected bimodal resonant behavior of

the microscanner and the competence of the proposed methodology to automatically design microscanners that operates at a specific resonant frequency and having a rotation axis located at the center of the mirror plate. The results also verify the precision of the analytical equations to describe the modal behavior of the microscanner.

Table 8. Comparison between high-level specifications and results obtained by analytical modeling and by FEM simulation.

Position of rotation axis at second resonance, r_2 (μm)		
High-level specification	Analytical solution	FEM simulation
428.87	428.87	428.86
Resonant frequency, f_n (kHz)		
High-level specification	Analytical solution	FEM simulation
--	7.96	8.14
50.00	49.88	49.81

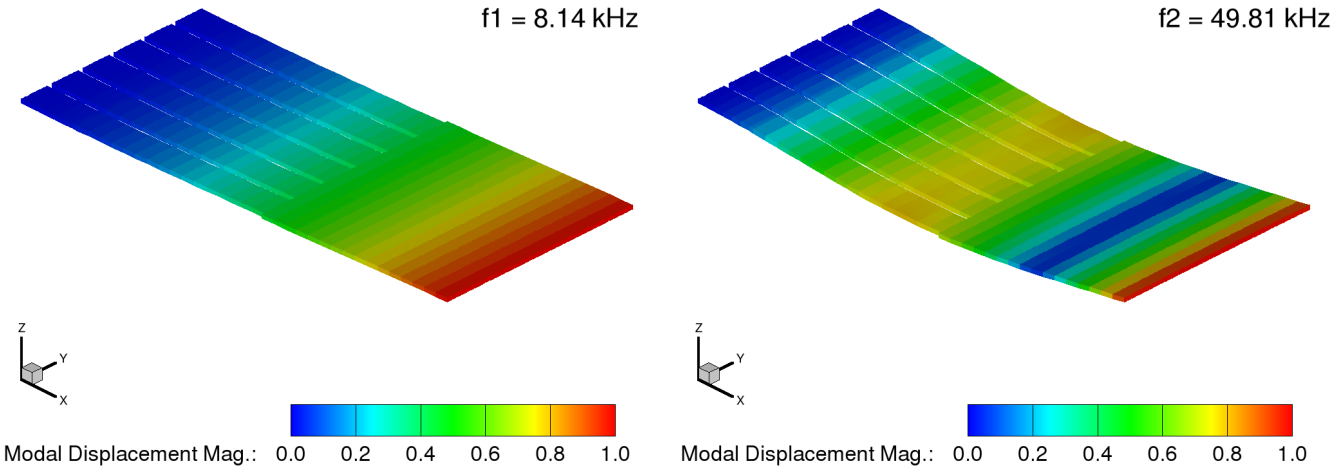

Figure 8. Dynamic shape deformation for the: (a) first and (b) second mode of vibration.

Conclusions

A structured design methodology for the gradual layout synthesis of a CMOS-compatible resonant scanning micromirror with out-of-plane electrothermal actuation and two accessible scanning modes has been demonstrated in this paper.

The design methodology consists of procedures for analytical thickness optimization and automatic layout synthesis. Thickness optimization allowed the maximum thermal sensitivity of the device and layout synthesis enabled the automatic generation of optimal and feasible layout configurations from high-level specifications. Scanning at second resonance permitted to simultaneously achieve a high scan frequency at resonance and a high rotation angle during static operation and additionally to maintain stationary the reflection point. A synthesized microscanner for OCT/OCM applications confirmed the fulfillment of the fabrication constraints of a standard CMOS process as well as the high-level specifications for position of rotation axis at second resonance and scan frequency with an error of less than 0.4% in both cases. The

analytical equations describe the device performance with maximum errors of 12.82% and 2.21% during static and dynamic operation, respectively.

Further development of this work will focus on the creation of macromodels to simulate the microscanner at the system level with the intention to investigate its capability to produce two-dimensional scanning patterns.

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